## REMARKS

Applicant is in receipt of the Office Action mailed March 12, 2004.

**Rejections Under Section 103**

Claims 1-5 and 8-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Poole et al. U.S. Patent 5,798,767 (hereafter referred to as Poole).

Claims 6 and 7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Poole et al. U.S. Patent 5,798,767 in view of Buckley et al. U.S. Patent 6,104,836 (hereafter referred to as Buckley).

Claim 1 as amended recites the limitations:

A reconfigurable circuit capable of performing a multitude of graphics data transforming operations, said circuit comprising:
a set of circuit elements comprising:
a subtractor coupled to receive a first input and a second input;
a multiplier coupled to a third input and an output of the subtractor;
an adder coupled to a fourth input and an output of the multiplier;
a first multiplexor whose output drives the first input;
a second multiplexor whose output drives the second input;
a third multiplexor whose output drives the third input; and
a fourth multiplexor whose output drives the fourth input;
an operation register, wherein a set of one or more values stored in the operation register specifies a specific graphics data transforming operation; and
control logic configured to implement a configuration of the circuit elements corresponding to the operation specified in the operation register, and to drive selection lines of the first, second, third and fourth multiplexors in response to the set of one or more values in the operation register.

A reconfigurable system and a reconfigurable circuit are described in Applicant's patent application on page 1, line 21 through page 2, line 9:

> "In one set of embodiments, a reconfigurable system for performing a set of arithmetic operations may be configured as follows. The reconfigurable system may include a frame buffer, a texture buffer and a pixel computation unit (e.g. a pixel transfer unit). The frame buffer may include an image buffer. The texture buffer may include an accumulation buffer. The pixel computation unit may include a control unit and one or more copies of a reconfigurable circuit.
>
> The reconfigurable circuit may include a subtractor, a multiplier, an adder, and a set of multiplexors. The control logic drives select lines of the set of multiplexors in the one or more circuit copies through one or more computational cycles in order to implement a programmable operation. The pixel computation unit may receive pixels values (or more generally, data values) from one or more sources including the frame buffer and the texture buffer, and operate on the pixels using the one or more circuit copies to generate a stream of output pixels.
>
> The reconfigurable system may also include one or more circuit elements, devices or subsystems configured to transfer the stream of output pixels to a programmable destination. For example, the programmable destination may be the accumulation buffer or the image buffer.
>
> The programmable operation may include one or more of the following operations: an addition operation, a multiply operation, an accumulate operation, a dynamic blending operation, a matrix-vector multiplication, a load operation and a return operation. The matrix-vector multiplication may be useful for color-space conversions."

Poole neither teaches nor suggests using a reconfigurable circuit to perform multiple operations on graphics data. Figure 4 of Poole clearly shows a pixel pipeline

that uses six separate single purpose circuits to perform six different graphics data operations. In fact, the word reconfigure is not used anywhere in Poole.

Amended claim 8 and new claim 12 contain limitations similar to claim 1 that are not taught or suggested by Poole either singly or in combination with Buckley. Therefore, claims 1, 8, and 15 and their dependents are patentably distinguished over Poole and Buckley for at least the reasons given above.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5681-13900/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

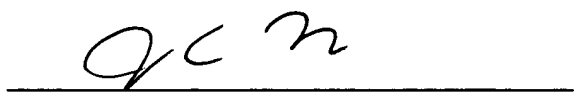
☐ Request for Approval of Drawing Changes

☒ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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